

A 802.11a WLAN Driver Amplifier using the Agilent Enhancement Mode PHEMT ATF-54143 Transistor

Application Note 1286

Introduction

Systems using the IEEE 802.11a standard will soon appear on the market to take advantage of higher data rates and more frequency channels for even greater performance. Typical first generation integrated solutions offer the up/down converter and modulator/demodulators on one chip and a base-band processing function on a second chip. This leaves a requirement for a discrete external power amplifier, low noise amplifier and switching function.

The driver amplifiers described in this application note are for use in applications covering 5.0 GHz to 5.8 GHz. This frequency range includes USA U-NII lower band 5.125 - 5.250 GHz, USA U-NII middle band 5.250 - 5.350 GHz and USA U-NII upper band 5.725 - 5.825 GHz. The focus will be on

the design considerations as well as the expected and actual performance. The paper contains six sections:

- 1) Design Goals
- 2) Device Selection
- 3) 5.125 - 5.325 Amplifier design
- 4) 5.725 - 5.825 Amplifier design
- 5) Test Results
- 6) Conclusions

Design Target

The primary target for the driver amplifier was to achieve 18 dBm P-1dB output power, adequate gain, and stability. For the 802.11a WLAN application, high intercept point, 5 volts and 3.3 volts supply voltage, and low current consumption are also required. The design goals were thus chosen as shown in Table 1 for both bands.

Device Selection

The Agilent ATF-54143 is an enhancement mode device and thus does not require a negative gate voltage. As shown later in the paper this simplifies the layout and reduces the parts count as compared to a depletion mode device.

The ATF-54143 is one of a family of new high dynamic range, low noise enhancement mode PHEMT devices designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. It has an 800-micron gate width with 2 GHz performance tested and guaranteed at a V_{ds} of 3 V and I_d of 60 mA. The Agilent ATF-54143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package. The enhancement mode ATF-54143 will only require one regulated supply. If active bias is desirable for repeatability of bias setting, then the ATF-54143 will only require the addition of a single PNP BJT. The circuit discussed in this note uses two PNP BJTs for enhanced stability at high temperatures.

Amplifier Design

Biasing Options and Source Grounding

In order to meet the design goals for P-1dB, intercept point and gain, the drain source current (I_{ds}) was chosen to be 80 mA. As indicated by the characterization data shown in the device data

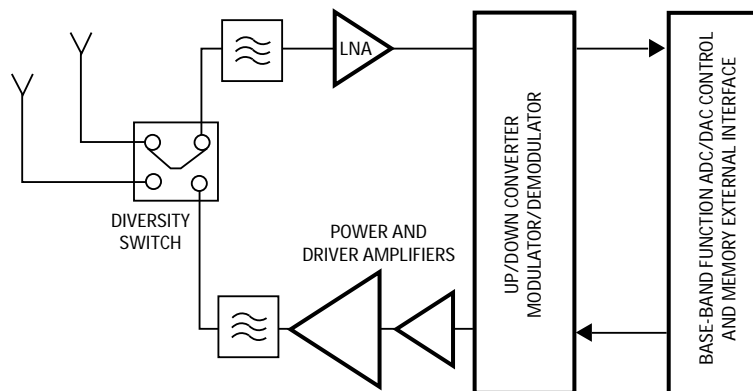


Figure 1. 802.11a Functional Block Diagram



Table 1. Design Goals

Parameter	Value
Gain	9.0 - 10.0 dB
Output 3rd Order Intercept Point	> 33 dBm
Input 3rd Order Intercept Point	> 23 dBm
Output P-1dB Compression	> 18 dBm
Input return loss	> 10 dB
Output return loss	> 10 dB
Supply Current	80 mA

sheet, 80 mA gives the target P-1dB of 18 dBm.

As mentioned earlier, one of the advantages of the enhancement mode PHEMT is the ability to dc ground the source's leads and yet only require a single positive polarity power supply. A depletion mode PHEMT pulls maximum drain current when $V_{gs} = 0$ V whereas an enhancement mode PHEMT pulls nearly zero drain current when $V_{gs} = 0$ V. The gate must be made positive with respect to the source for the enhancement mode PHEMT to begin pulling drain current. It is also important to note that if the gate terminal is left open circuited, the device will pull some amount of drain current due to leakage current creating a voltage differential between the gate and source terminals.

A suggested active biasing circuit is shown in Figure 2. The active biasing scheme uses the BCV62B current mirror bias circuit. The BCV62B has two PNP transistors in the same package; Q3 has the base and collector connected internally to the base of Q2. It behaves as a two-terminal pn diode, the voltage drop across the pn junction is typically 0.6 volts. The EB junction of Q3 is forward biased by exactly the same voltage as the EB junction of Q2. The two bipolars are operating like a volt-

age comparator, with the gate bias being adjusted to keep the voltages across R5 (and therefore I_d and V_{ds}) equal to the voltage across R4 which is determined by the potential divider R4, Q3Vbe and R6. Including the Q3Vbe junction in the potential divider chain temperature compensates Q2Vbe assuming the currents in the two PNP transistors are approximately equal. More details on active bias circuits may be found in references [4] and [5].

$$R6 \approx \frac{V_{DS} - Q2V_{be}}{I_{REF}}$$

$$R4 \approx \frac{V_{DD} - V_{DS}}{I_{REF}}$$

$$R5 \approx \frac{V_{DD} - V_{DS}}{I_{DS}}$$

Where:

I_{DS} is the desired drain current.

I_{REF} is the current flowing through the R6.

I_{REF} was chosen to be 2.0 mA for the 5 V design and 1.0 mA for the 3.3 volt design.

$V_{DD} = 5$ V, $V_{DS} = 3$ V, $I_{DS} = 80$ mA,

$V_{gs} = 0.6$ V

$R6 = 1200$ Ω

$R2 = 1000$ Ω

$R3 = 1000$ Ω

$R4 = 1000$ Ω

$R5 = 25$ Ω

R2 and R3 act as a potential divider circuit with a ratio of 1:1, two 1k ohm resistors were chosen. The collector voltage of Q2 should be $2 \times V_{gs}$.

An active bias circuit using a single PNP BJT is discussed in [1]. A passive bias circuit is also discussed in [1].

The component parts list for the two amplifiers is shown in Table 3. Figures 7 and 8 show the component placement and the RF layout.

The use of a controlled amount of source inductance can often be used to aid stability at the cost of reducing gain. The amount of inductance required is usually only a few tenths of a nano-henry. This is effectively equivalent to increasing the source leads by only 0.030 inch or so. The effect can be easily modelled using a RF simulation tool such as Agilent Technologies' *Advanced Design System* (ADS). The usual side effect of excessive source inductance is very high frequency gain peaking and resultant oscillations. The larger gate width devices have less gain at high frequency and therefore the high frequency performance is not as sensitive to source inductance as a smaller gate width device would be.

ATF-54143 Driver Amplifier Design Using Agilent Technologies' EEs of Advanced Design System Software the amplifier circuit can be simulated in both linear and non-linear modes of operation. The original design draft was a driver amplifier with a P-1dB of 18 dBm and an Output Third Order Intercept Point (OIP3) of 35 dBm at 5 - 6 GHz.

Linear Analysis

For the linear analysis the transistors can be modelled with a

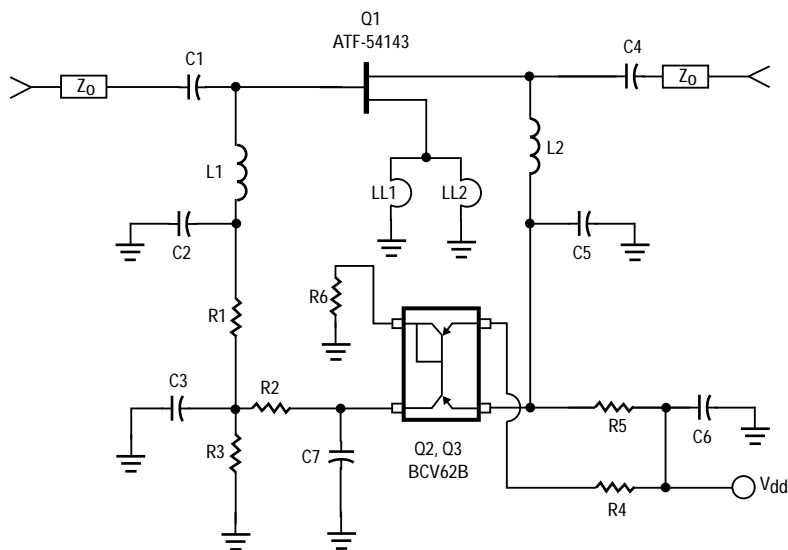


Figure 2. The Amplifier Schematic

two port s-parameter file using Touchstone™ format. The ATF54143.s2p file can be downloaded from the Agilent Wireless Design Center web site. The simulation controls can be obtained from the Spams_wNoise template available in ADS. The circuit components can then be added to the simulation circuit. The more detailed the simulation the more accurate the results will be. An accurate circuit simulation can provide the appropriate first step to a successful amplifier design. Transmission line section can be modelled with various micro-strip and strip-line elements available in the component library. In this case, all micro-strip sections assumed a 0.010 inch thick board and FR-4 material. The inductance associated with the chip capacitors and resistors was also included in the simulation. Where possible, models were chosen from the ADS SMT component library. Models of SMT components can also be obtained from the manufacturers' web sites. Manufacturing tolerances in both the active and passive components often prohibit perfect

correlation. When the design met the target specifications for gain, noise figure and stability, the create/edit schematic symbol function was used from the view menu in ADS. This allows the designer to easily duplicate the amplifier design.

The results of the simulated gain, input and output return losses are

shown in Figures 3 and 4. The linear simulated performance of the amplifier was close to the measured results.

As noted on the data sheet, the ATF-54143 S and Noise Parameters are tested in a fixture that includes plated through holes through a 0.025 " thickness printed circuit board. Due to the complexity of de-embedding these grounds, the S and Noise Parameters include the effects of the test fixture grounds. Therefore, when simulating a 0.010" thickness printed circuit board, the reduced amount of inductance in the ground path had to be taken into account. The transmission lines that connect each source lead to its corresponding plated through hole is simulated as a microstrip transmission line (MLIN).

Non-linear Analysis

For the non-linear analysis, a harmonic-balance (HB) simulation was used. HB is preferred over other non-linear

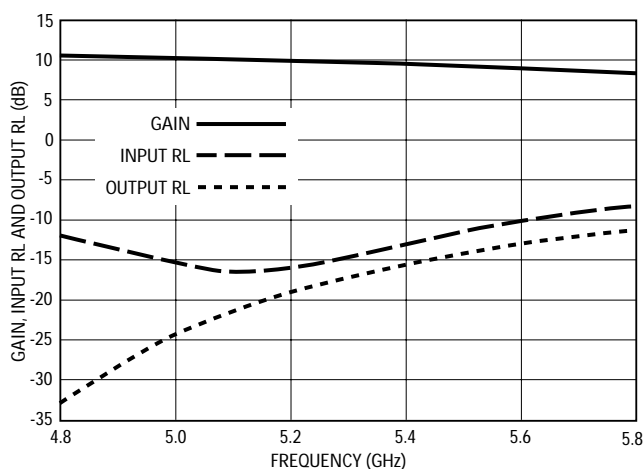


Figure 3. Linear Simulated Gain, Input and Output Return Loss vs. Frequency for 5.125 - 5.325 GHz band amplifier

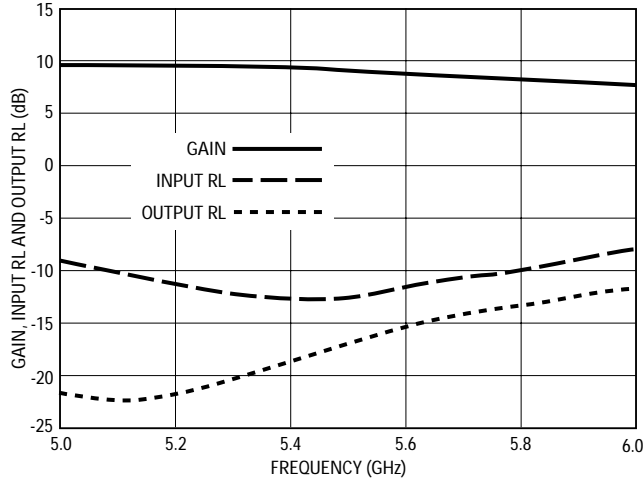


Figure 4. Linear Simulated Gain, Input and Output Return Loss vs. Frequency for 5.725 - 5.825 GHz band amplifier

methods because it is computationally fast, handles both distributed and lumped element circuitry, and can easily include higher-order harmonics and inter-modulation products [2]. In this application HB was used for simulation of 1 dB compression point (P-1dB) and output third order intercept point (OPI3).

The non-linear transistor model used in the simulation is based on the work of Curtice [3]. The model can be downloaded from Agilent's web-site. An important feature of the non-linear model is the use of a quadratic expression for the drain current versus gate voltage. Although this model closely predicts the DC and small signal behaviour (including noise), it does not predict the intercept point correctly. For example, the

amplifier OIP3 was simulated at +31.7 dBm and the P-1dB at +18.0 dBm. The simulated performance for P-1dB was very close to the measured results, however, the simulated OIP3 was too low. (See Table 2). To properly model the exceptionally high linearity of the E-pHEMT transistor, a better model is needed. This model, however, can still be used to predict the relative importance of output matching, bias, and source inductance.

Circuit Stability

Besides providing important information regarding gain, P-1dB, noise figure, input and output return loss, the computer simulation provides very important information regarding circuit stability. Unless a circuit is actually oscillating on the bench, it may be difficult to predict

instabilities without actually presenting various VSWR loads at various phase angles to the amplifier. Calculating the Rollett Stability factor K and generating stability circles are two methods made considerably easier with computer simulations.

The simulated gain and input/output return loss of the ATF-54143 amplifier are shown in Figures 3 and 4. These plots only address the performance near the actual desired operating frequency. It is still important to analyze out-of-band performance in regards to abnormal gain peaks, positive return loss and stability. A plot of Rollett Stability factor K as calculated from 1 GHz to 12 GHz is shown in Figure 5 for the amplifier. Source inductance can be used to help stability. However, it should be noted that excessive inductance will cause high frequency stability to get worse (i.e., decreased value of K).

Final ATF-54143 Amplifier Design

As discussed previously, the amplifier was designed for a V_{ds} of 3 volts and an I_{ds} of 80 mA. The amplifier schematic is shown in Figure 2. Two bias designs are discussed:

- 1) the 5.125 - 5.325 GHz amplifier uses a power supply voltage, V_{dd} , of 3.3 V.
- 2) the 5.725 - 5.825 GHz amplifier uses a power supply voltage, V_{dd} , of 5.0 V.

The evaluation board shown in Figure 6 is used for both designs. The board gives the designer two design options for the RF circuitry. The evaluation board was designed such that the input and output impedance matching networks can be adjusted to optimize the performance over the 5 - 6 GHz frequency range.

Table 2. Simulated non-linear performance

Bias Conditions	P-1dB	Third Order Intercept
3V, 60 mA	16.8 dBm	31.4 dBm
3V, 80 mA	18.0 dBm	31.7 dBm

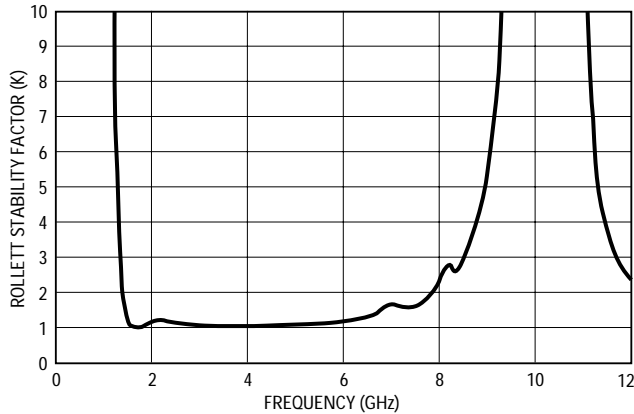


Figure 5. Simulated Rollett Stability Factor K

Either lumped element inductors or printed microstrip high impedance lines can be used as matching networks. The lumped inductors allow a more compact design at an increase in cost. The demo board is etched on 0.031" thickness, multi-layer FR-4 material for cost considerations. The distance between the RF layer and the first ground layer is 0.010".

The amplifier uses a high-pass impedance matching network for the noise match. The high-pass network consists of a series capacitor C1 and shunt inductor L1. The circuit loss will directly relate to noise figure, thus Q of L1 is extremely important. The Johanson L-07C3N9KT or similar device is suitable for this purpose. The Johanson L-07C3N9KT is a small multi-layer chip inductor with a rated Q of 30.7 at 1.8 GHz. C1 also doubles as a dc block. L1 also doubles as a means of inserting gate voltage for biasing up the PHEMT. This requires a good bypass capacitor in the form of C2. This network has been used to optimize the input return loss and gain. Resistor R2 and capacitors C2 and C4 provide in-band stability while resistors R1 and R3 provide low frequency stability by providing a resistive termination. The high-pass

network on the output consists of a series capacitor C4 and shunt inductor L2. L2 also doubles as a means of inserting drain voltage for biasing up the PHEMT. The parts list for both amplifiers is shown in Table 3. The artwork and component placement are shown in Figures 7 and 8.

Inductors LL1 and LL2 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demo board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstrip section, which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad is connected to the ground pad with a very short piece of etch at the point closest to the device source lead. For the amplifier, each source lead is connected to its corresponding ground pad at a distance of approximately 0.032" from the source lead. The 0.032" is measured from the edge of the source lead to the closest edge of the first via hole. This is discussed in detail in the next section.

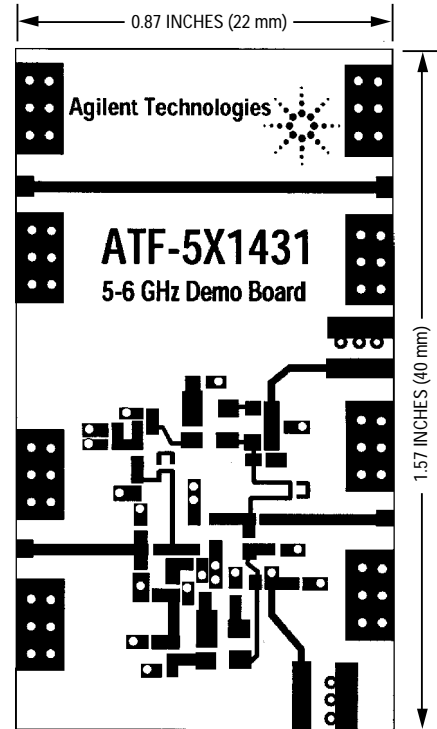


Figure 6. Artwork for the ATF-54143 Driver Amplifier

Determining the Optimum Amount of Source Inductance

As mentioned previously, adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential downside is reduced low frequency gain. However, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone to far? Normally the high frequency gain roll-off will be gradual and smooth. Adding source inductance begins to add bumps to the once smooth roll-off. The source inductance, while having a degenerative effect at low frequencies, is having a regenerative effect at higher frequencies. This shows up as a gain peak in S21 and also shows up as input return loss S11 becoming more positive. Some

Table 3. Component Parts List for the ATF-54143 Amplifier

Frequency	5.125 - 5.325 GHz, 3.3 V Demo circuit	5.725 - 5.825 GHz, 5.0 V Demo circuit
C1	0.8 pF Johanson S402D chip capacitor	0.5 pF Johanson S402D chip capacitor
C2, C5	5.6 pF Johanson S402D chip capacitor	5.6 pF Johanson S402D chip capacitor
C3, C6, C7	10000 pF chip capacitor	10000 pF chip capacitor
C4	1.8 pF Johanson S402D chip capacitor	2.2 pF Johanson S402D chip capacitor
LL1, LL2	Source inductance of width 25 mil x length 32 mil microstrip between source and first via hole can be used to increase stability.	Source inductance of width 25 mil x length 32 mil microstrip between source and first via hole can be used to increase stability.
L1, L2	3.9 nH Johanson L-07C3N9KT chip inductor	Printed 280 x 10 mil microstrip line
R1	47 Ω	47 Ω
R2, R3	1000 Ω	1000 Ω
R4	300 Ω	1000 Ω
R5	4 Ω	25 Ω
R6	2400 Ω	1200 Ω
Q1	Agilent Technologies ATF-54143	Agilent Technologies ATF-54143
Q2, Q3	BCV62B, Philips or Infineon	BCV62B Philips or Infineon

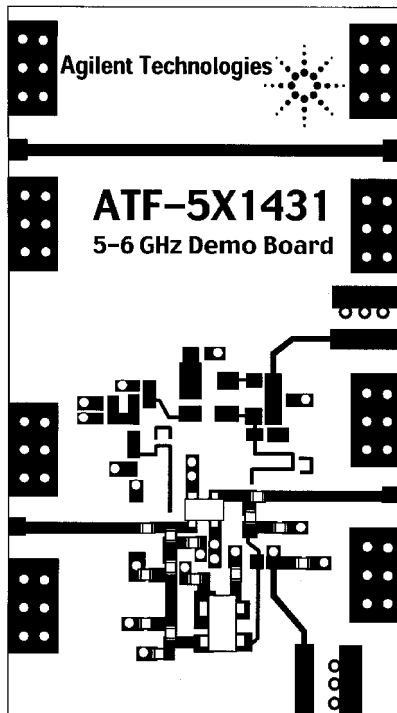


Figure 7. Component Placement Drawing for the 5.125 - 5.325 GHz ATF-54143 Driver Amplifier

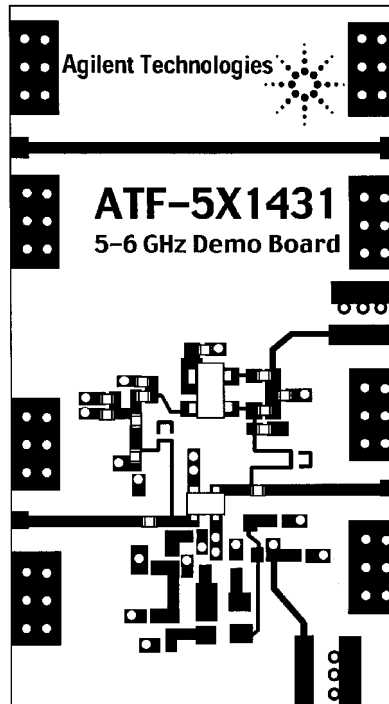


Figure 8. Component Placement Drawing for the 5.725 - 5.825 GHz ATF-54143 Driver Amplifier

shift in upper frequency performance is fine as long as the amount of source inductance is fixed and has some margin in the design in order to account for S21 variations in the device.

Figure 6 shows the artwork of the top RF layer of the ATF-5X143 evaluation board. The second layer is the groundplane and includes the dc connections required for the biasing network, the thickness between the top layer and second layer is 0.010". A third layer, which is also a groundplane, a further 0.010" down, makes up the additional material thickness and adds to the mechanical stability of the board, making the board a total of 0.031" thick. A 50 ohm line has been included on the board to aid the amplifier design. The 50 ohm line can also be used as a quick check that the board has been accurately manufactured. The 50 ohm line was found to have 0.5dB insertion loss at 5.2 GHz, the return loss was measured at 23 dB. The Smith chart showed the board imped-

ance was centered on 50 ohms. Capacitors and inductors being considered can be placed on the line to check to see if they are self-resonant in the amplifier bandwidth. This could be a potential problem.

Test Results

Performance of the 5.125 - 5.325 GHz ATF-54143 Amplifier

The amplifier is biased at a V_{ds} of 3 volts and I_d of 80 mA, from a 3.3 volts supply. Typical V_{gs} is 0.6 volts. The complete amplifier is shown in Figure 7. The measured input and output return loss and gain of the completed amplifier are shown in Figure 9. Gain is typically 9.5 dB at 5.2 GHz. The input return loss at 5.2 GHz is 12 dB with a corresponding output return loss of 8.5 dB. The amplifier output intercept point (OIP3) was measured at a nominal +34 dBm at a dc bias point of 3 volts V_{ds} and an I_d of 80 mA. P-1dB measured +19.8 dBm. The amplifier was additionally tested under the following conditions:

16QAM octets = 516, code rate = 1/2, bit rate = 24 Mbps. It was found to exceed the -16 dB EVM specification for 24 Mbps at 7 dBm input power level. This corresponds to an output power level of 16.5 dBm.

Performance of the 5.725 - 5.825 GHz ATF-54143 Driver Amplifier

The amplifier is biased at a V_{ds} of 3 volts and I_d of 80 mA, from a 5 volts supply. Typical V_{gs} is 0.6 volts. The complete amplifier is shown in Figure 8. The measured gain, input and output return loss of the completed amplifier are shown in Figure 10. Gain is typically 9.3 dB at 5.7 GHz. The input return loss at 5.7 GHz is 19 dB with a corresponding output return loss of 10.0 dB. The

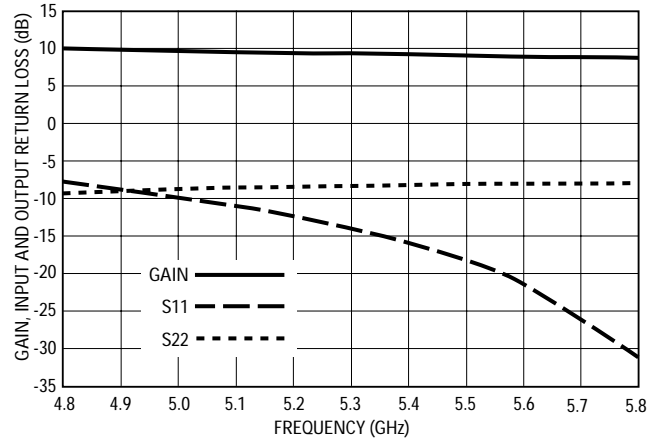


Figure 9. Measured Performance of the 5.125 - 5.325 GHz ATF-54143 Driver Amplifier

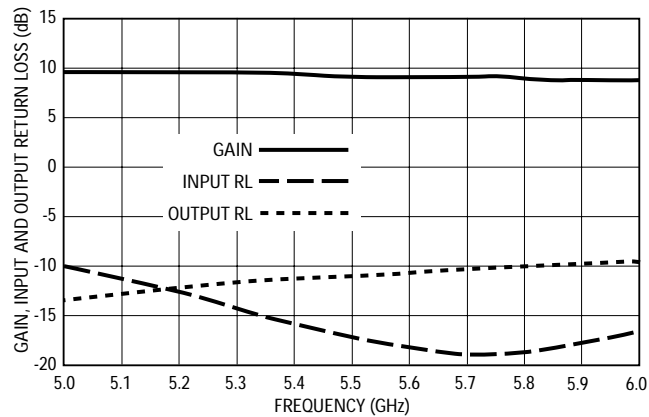


Figure 10. Measured Performance of the 5.725 - 5.825 GHz ATF-54143 Driver Amplifier

amplifier output intercept point (OIP3) was measured at a nominal +33.5 dBm. P-1dB measured +19.6 dBm. The amplifier was additionally tested under the following conditions: 16QAM octets = 516, code rate = 1/2, bit rate = 24 Mbps. It was found to exceed the -16 dB EVM specification for 24 Mbps at 7 dBm input power level. This corresponds to an output power level of 16.3 dBm.

Conclusions

A driver amplifier design has been presented using the Agilent Technologies ATF-54143 low noise enhancement mode PHEMT. The ATF-54143 provides 19 dBm P-1dB along with high intercept point making it ideal for applications where high dynamic range is required. It also has the advantage of a single polarity bias. The use of simulation to predict performance before fabricating the prototype led to first time success. The models for the transistor, microstrip line, and the lumped elements, led to excellent agreement between modeled and measured thus confirming the validity of the simulations.

References

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Performance data for ATF-54143 PHEMT may be found on
<http://www.agilent.com/view/rf>

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June 5, 2002
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套装包含 4 门视频培训课程,培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合,全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作,同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习,可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试...

详情浏览: <http://www.edatop.com/peixun/antenna/116.html>



我们的课程优势:

- ※ 成立于 2004 年,10 多年丰富的行业经验,
- ※ 一直致力并专注于微波射频和天线设计工程师的培养,更了解该行业对人才的要求
- ※ 经验丰富的一线资深工程师讲授,结合实际工程案例,直观、实用、易学

联系我们:

- ※ 易迪拓培训官网: <http://www.edatop.com>
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